**Department Of Mathematics**

**Ahmadu Bello University, Zaria**

**First Semester Examination 2009/2010 Session**

**COSC303: Introduction to Computer Architecture**

**Instructions: Answer Any Four Questions. Time Allowed: 2 Hours**

* 1. Almost all computer hardware courses include a section on data representation and the conversion of numbers between bases. Does the base in which a computer represents numbers really matter to the computer scientist?
  2. Suppose that we want to enhance the processor used for Web serving. The new processor is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 70% of the time and is waiting for I/O 30% of the time.

i. What is the overall speedup gained by incorporating the enhancement?

ii. What is the efficiency?

* 1. Consider a machine with three instruction classes and CPI measurements as shown in (a). Suppose that we measured the code for a given program in two different compilers and obtained the data in (b):

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Instruction Class | CPI of the instruction class | | A | 2 | | B | 5 | | C | 7 |   (a) | |  |  |  |  | | --- | --- | --- | --- | | Code Sequence | Instruction counts(in millions) | | | | A | B | C | | Compiler1 | 15 | 5 | 3 | | Compiler 2 | 25 | 2 | 2 |   (b) |

Assume that the machine’s clock rate is 500 MHz, Which code sequence will execute faster :

* + 1. According to MIPS?
    2. According to execution time?

1. What argument do you have for or against the following statement:”using a faster processor chip results in a corresponding increase in performance of a computer, even if the main memory speed remains the same.”
2. What do you understand by the following terms with respect to computer memories: capacity, cycle time, latency, bandwidth
3. Consider a non-pipelined machine with 6 execution stages of lengths 20 ns, 50 ns, 60 ns, 65 ns, 20 ns, and 50 ns.
   * 1. Find the instruction latency of this machine
     2. How much time does it take to execute 1000 instructions?

Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock skew adds 4ns of overhead to each execution stage

* + 1. What is the instruction latency on the pipelined machine?
    2. How much time does the pipelined machine take to execute 1000 instructions?
    3. Calculate the speedup obtained by introducing pipelining on this machine
  1. Describe write-through and write-back cache write policies. Discuss their performance advantages and disadvantages.
  2. Many instruction sets contains the instruction NOOP, meaning no operation, which has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction
  3. Let T=1/5 denotes the fraction of time that must be spent on the sequential parts of a program Q and let P=4/5 denotes the fraction of time spent on the parallelized parts of Q.
     1. By using the Amdahl’s law, calculate the speedup S(n) achievable by n-processor computer executing Q.
     2. For n=10 processors computer, calculate the efficiency of executing Q on this computer
        1. Define the terms "spatial locality" and "temporal locality", and explain how caches are used to exploit them for a performance benefit.
        2. Compare one and two address format machines by writing the statement code to compute X=(A+B\*C)/(D - E\*F)
        3. Consider the execution of the following sequence of instructions on a five-stage pipeline consisting of IF, ID, OF, IE, and IS.

|  |  |
| --- | --- |
| Instruction number | Instruction |
| 1 | Load -1,R1 |
| 2 | Load 5,R2 |
| 3 | Sub R2,1,R2 |
| 4 | Add R1,R2,R3 |
| 5 | Add R4,R5,R6 |
| 6 | Shift R3 |
| 7 | Add R6,R4,R7 |

1. Identify all the data dependencies and their type between those instructions
2. By using the Gantt’s chart illustrates the progression of these instructions in the pipeline taking into consideration the data dependencies identified in (i) above.
3. Define the terms "structural hazard", "control hazard", and "data hazard" in the context of pipelines. Which of these hazards is addressed by a hardware branch predictor (which guesses whether a branch will be taken or not)? For one of the other hazards, suggest a way, either in software or hardware, how the effect of that hazard could be reduced
4. State five differences between RISC and CISC architecture.
5. Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 2GHZ.

|  |  |  |
| --- | --- | --- |
| Instruction Category | Percentage of occurrence | No. of cycle per instruction |
| ALU | 20% | 1 |
| Branch | 45% | 4 |
| Load & store | 20% | 2 |
| Others | 15% | 3 |

* 1. Evaluate the overall CPI.
  2. Calculate the CPU time needed to execute 1000 instructions

1. One approach to reducing cache miss rate is to increase cache block size. Briefly explain how doing so might affect the miss penalty.
2. A computer has a cache, main memory and a disk used for virtual memory. If a referenced word is in the cache, 20ns are required to access it. If it is in main memory but not in the cache, 60ns are needed to load it into the cache and then the reference is started again. If the word is not in main memory, 12000ns are required to fetch the word from disk, followed by 60ns to copy it to the cache and then the reference is started again. The cache hit ratio is 0.9 and the main memory hit ratio is 0.6. what is the average time in ns required to access a referenced word on this system
3. Given a processor with 7 stages pipeline that, if a branch is taken, then 6 cycles are required to flush the pipeline. This processor is used to execute program P in which, the probability that an instruction is a branch is 1/5 and the probability that the branch is taken is 1/2.
   1. Calculate CPI for the execution of this program on the pipelined machine.
   2. Calculate the execution efficiency.
   3. Calculate an average number of cycle require to execute 100 instructions.
   4. Assuming that the clock rate is 200MHZ, calculate the CPU time taken to execute 100 instructions