**Department of Mathematics**

**Ahmadu Bello University, Zaria**

**First Semester Examination 2012/2013 Session**

**COSC303: Introduction to Computer Architecture**

**Instructions: Answer Any Four Questions. Time Allowed: 2 Hours**

1. Using *n* bits, what is the largest and smallest integer that can be represented in the two’s complement system?
	1. What happens if the smallest number is
* Incremented
* Decremented
	1. What happens if the largest numbers is
* Incremented
* Decremented
1. Distinguish between overflow and carry when these terms are applied to two complement arithmetic on n-bit words
2. On a computer machine that doesn’t detect integer overflow in hardware, explain how you would detect overflow on a signed addition operation in software.
	1. Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 2GHZ.

|  |  |  |
| --- | --- | --- |
| Instruction Category | Percentage of occurrence | No. of cycle per instruction |
| ALU | 20% | 1 |
| Branch | 45% | 3 |
| Load & store | 20% | 4 |
| Others | 15% | 3 |

1. Evaluate the overall CPI.
2. Calculate the CPU time needed to execute 1000 instructions
	1. Consider having a program that runs in 50 ns on computer A, which has a 3GHz clock rate. We would like to run the same program on another machine, B, in 20 ns. If machine B requires 2 times as many clock cycles as machine A for the same program, what clock rate must machine B have in GHz?
		* 1. Consider the execution of the following sequence of instructions on a five-stage pipeline consisting of instruction fetching (IF), instruction decoding(ID),operand fetching(OF),instruction execution(IE) and result storing( IS).

|  |  |
| --- | --- |
| Instruction number | Instruction |
| 1 | Load -1,R1 |
| 2 | Load 5,R2 |
| 3 | Sub R2,1,R2 |
| 4 | Add R1,R2,R3 |
| 5 | Add R4,R5,R6 |
| 6 | Add R6,R4,R7 |

1. Identify all the data dependencies and their type between those instructions
2. By using the Gantt’s chart illustrates the progression of these instructions in the pipeline taking into consideration the data dependencies identified in (i) above.
3. What is the speedup?
	* + 1. Consider a pipelined machine with the execution stages of lengths 60ns, 50ns, 60ns, 50ns and 30ns
		1. Find the instruction latency of this machine
		2. How much time does it take to execute 1000 instructions?
		3. Calculate the speedup obtained by introducing pipelining on this machine
	1. Suppose that we want to enhance the processor used for Web serving. The new processor is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 70% of the time and is waiting for I/O 30% of the time.
		1. What is the overall speedup gained by incorporating the enhancement?
		2. What is the efficiency?
	2. Let T=1/5 denotes the fraction of time that must be spent on the sequential parts of a program Q and let P=4/5 denotes the fraction of time spent on the parallelized parts of Q.
		1. By using the Amdahl’s law, calculate the speedup S(n) achievable by n-processor computer executing Q.
		2. For n=10 processors computer, calculate the efficiency of executing Q on this computer
4. Define the terms "spatial locality" and "temporal locality". Explain how caches are used to exploit them for a performance benefit by evaluating their impact in reducing the average memory access time
5. A computer has a memory hierarchy that consists of three levels: cache, main memory and a disk used for virtual memory. Let h1, h2, h3, be the hit ratio of cache, main memory and a disk respectively and Let t1, t2, t3 be the access time of cache, main memory and disk respectively.
6. Define an expression for the average memory access time of this system.
7. If t1=20ns, t2=30ns, t3=60ns and h1=60%, h2=80%, h3=100% what is the average time in ns required to access a referenced word on this system.
8. Explain what you understand by the following terms:
9. Memory cycle time
10. Memory access time
11. Memory bandwidth
12. Cache Coherency
13. Sequential access memory
14. Suppose you own a computer with 6-stage pipelining of equal length that exhibits the following properties on the programs that you run:
* The pipeline can accept a new instruction every cycle
* The cache can provide data every cycle (i.e. no penalty for cache hits)
* The cache miss rate is 2%
* 20% of instructions are memory instructions
* The cache miss penalty is 4 cycles.
1. What is the average number of cycle taken to execute 100 instructions?
2. If the computer frequency is 200MHZ, what is the average time in second required to execute 100 instructions on this system?