**Department Of Mathematics**

**Ahmadu Bello University, Zaria**

**First Semester Examination 2010/2011 Session**

**COSC303: Introduction to Computer Architecture**

**Instructions: Answer Any Four Questions. Time Allowed: 2 Hours**

1. Suppose that we have two implementations of the same instruction set architecture. Machine A has a clock cycle time of 50 ns and a CPI of 4.0 for some program, and machine B has a clock cycle of 65 ns and a CPI of 2.5 for the same program. Which machine is faster and by how much?
2. A computer has a cache, main memory and a disk used for virtual memory. If a referenced word is in the cache, 10ns are required to access it. If it is in main memory but not in the cache, 30ns are needed to load it into the cache and then the reference is started again. If the word is not in main memory, 1200ns are required to fetch the word from disk, followed by 30ns to copy it to the cache and then the reference is started again. The cache miss ratio is 0.5 and the main memory miss ratio is 0.3. What is the average time in ns required to access a referenced word on this system?
3. Consider having a program that runs in 50 s on computer A, which has a 500 MHz clock. We would like to run the same program on another machine, B, in 20 s. If machine B requires 2.5 times as many clock cycles as machine A for the execution of the same program, what clock rate must machine B have in MHz?
4. Consider the execution of the following sequence of instructions on a five-stage pipeline consisting of IF, ID, OF, IE, and IS.

|  |  |
| --- | --- |
| Instruction number | Instruction |
| 1 | Load -1,R2 |
| 2 | Load 5,R1 |
| 3 | Sub R2,1,R2 |
| 4 | Add R1,R2,R3 |
| 5 | Add R4,R5,R6 |
| 6 | Shift R3 |
| 7 | Add R6,R4,R7 |

1. Identify all the data dependencies and their type between those instructions
2. By using the Gantt’s chart illustrates the progression of these instructions in the pipeline taking into consideration the data dependencies identified in (i) above.
3. The controversy of RISC versus CISC never ends. Suppose that you represent an advocate for the RISC approach; state the critics of the CISC approach showing its disadvantages while showing the advantages of the RISC approach. You may want to use real-life example machine performance as a support for your support of the RISC philosophy.
4. A computer has a cache, main memory and a disk used for virtual memory. If a referenced word is in the cache, 1 cycle is required to access it. If it is in the main memory but not in the cache, 4 cycles are needed to load it into the cache and then the reference is started again. The probability that an instruction reference a memory is 0.2. The cache ratio is 0.7.
5. what is the average number of cycle taken to execute 100 instructions?
6. If the computer frequency is 2GHZ, what is the average time in second required to execute 100 instructions on this system?
7. Explain the concepts of write-through and write-back cache update policies and discuss their performance advantages and disadvantages.
8. Suppose that we want to enhance the processor used for Web serving. The new processor is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 80% of the time and is waiting for I/O 20% of the time.
9. What is the overall speedup gained by incorporating the enhancement?
10. What is the efficiency?
11. How many times should the new processor be faster on computation in the Web serving application than the original processor if we want to achieve a speedup of 4.
12. When a miss occurs, the cache controller must select a block to be replaced with the desired data. A replacement policy determines which block should be replaced. With fully-associative and set-associative placement, there are more than one block to choose from on a miss. State two replacement policies and discuss their advantages and disadvantages
13. Consider a non-pipelined machine with 5 execution stages of lengths 55 ns, 45 ns, 60 ns, 60 ns, and 20 ns.
	* 1. Find the instruction latency of this machine
		2. How much time does it take to execute 100 instructions?

Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock skew adds 4ns of overhead to each execution stage

* + 1. What is the instruction latency on the pipelined machine?
		2. How much time does the pipelined machine take to execute 100 instructions?
		3. Can we conclude that an increasing number of stages always provide increasing performance? (assuming that increasing the number of stages will not lead to structural hazard).
1. Define the terms "spatial locality" and "temporal locality", and explain how caches are used to exploit them for a performance benefit.
2. Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 1GHZ.

|  |  |  |
| --- | --- | --- |
| Instruction Category | Percentage of occurrence | No. of cycle per instruction |
| ALU | 30% | 1 |
| Branch | 35% | 2 |
| Load & store | 15% | 2 |
| Others | 20% | 3 |

* 1. Evaluate the overall CPI.
	2. Calculate the CPU time needed to execute 2000 instruction