Chapter 11

Introduction to Multiprocessors

11.1 Introduction

- A multiple processor system consists of two or more processors that are connected in a manner that allows them to share the simultaneous (parallel) execution of a given computational task.
- Two basic requirements are inevitable for the efficient use of the employed processors. These requirements are:
  - Low communication overhead among processors while executing a given task and
  - A degree of inherent parallelism in the task.

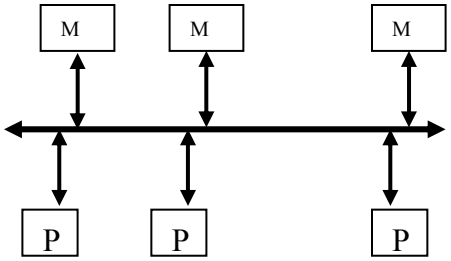
11.1 Introduction

- Typical sizes of some multiprocessor systems:

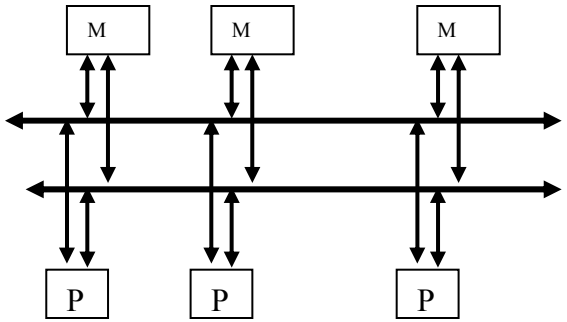
Category	Sub-categories	Number of processors
Communication Model	Multiple Processors	2-256
	Multiple Computers	8-256
Physical Connection	Bus-based	2-32
	Network-based	8-256

11.1 Introduction

- The organization and performance of a multiple processor system are greatly influenced by the interconnection network used to connect them.
  - Single bus

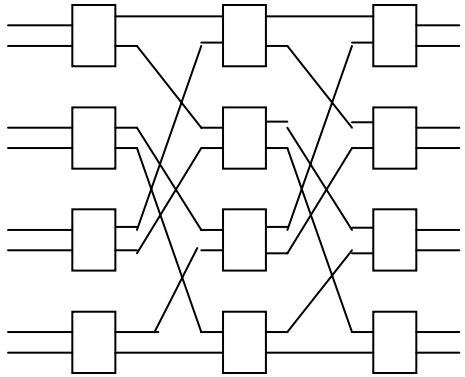


  - Multi-bus system

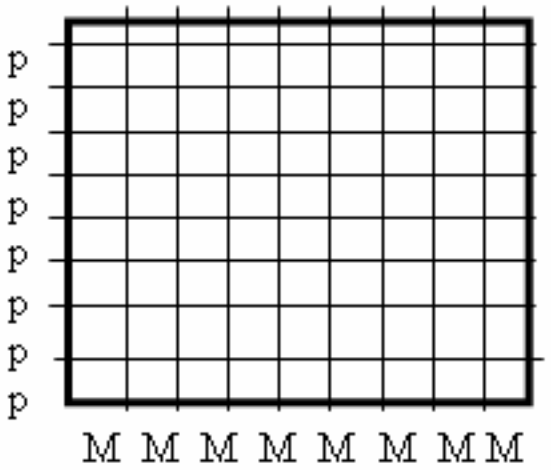


11.1 Introduction

– Multi-stage Interconnection Network

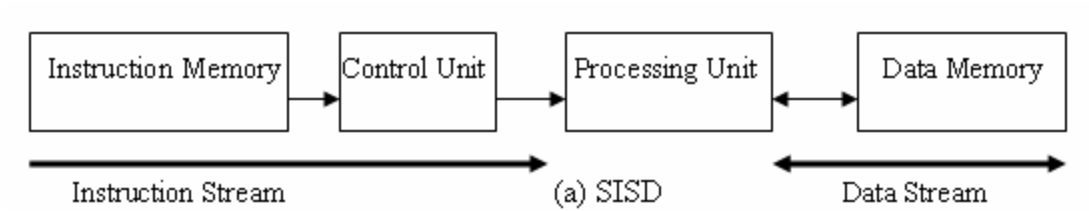


– Crossbar system

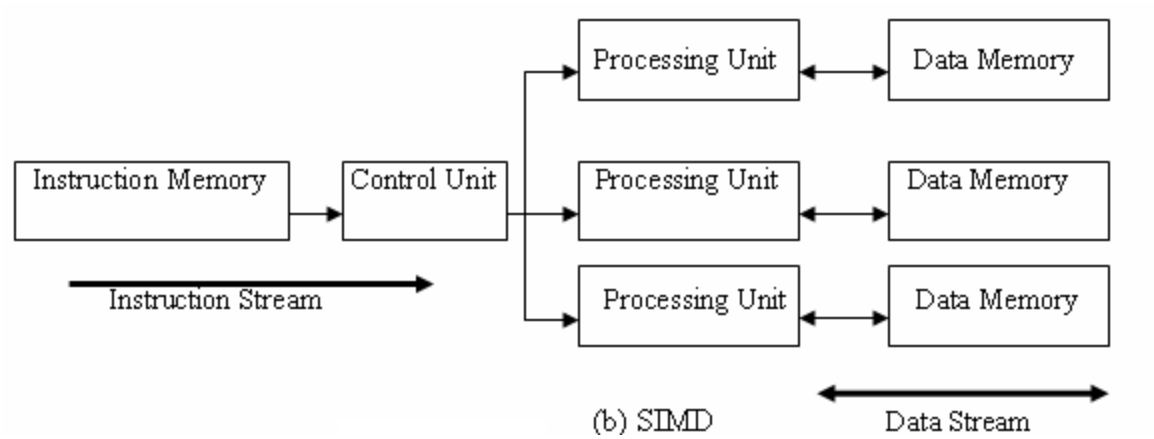


11.2 Classification of Computer Architectures

- Flynn's Classification:
  - SISD:

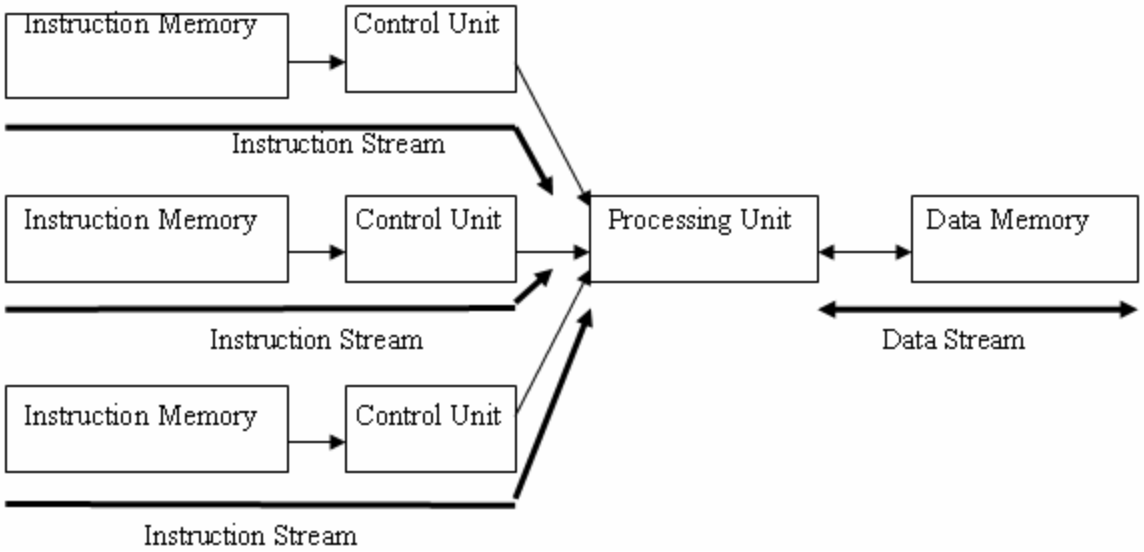


  - SIMD:

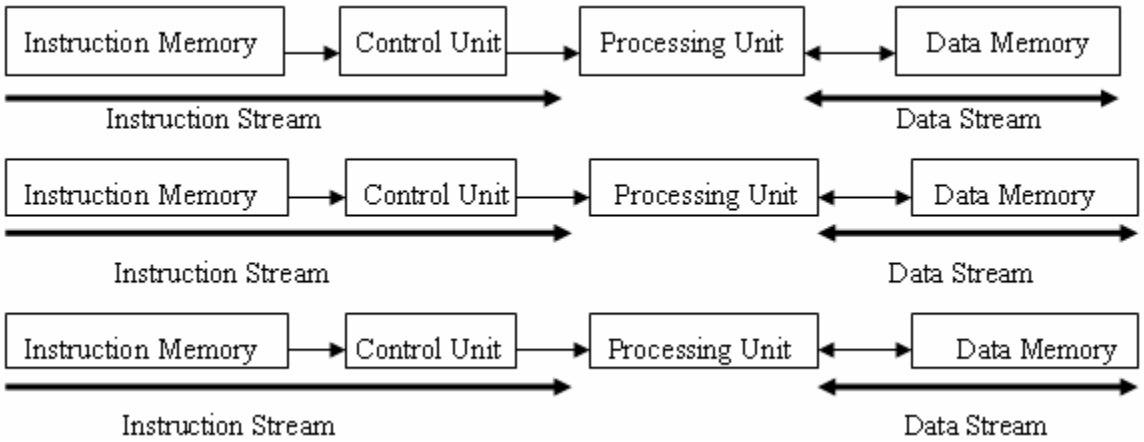


11.2 Classification of Computer Architectures

- Flynn's Classification:
  - MISD:



  - MIMD:



11.2 Classification of Computer Architectures

- Kuck Classification Scheme:

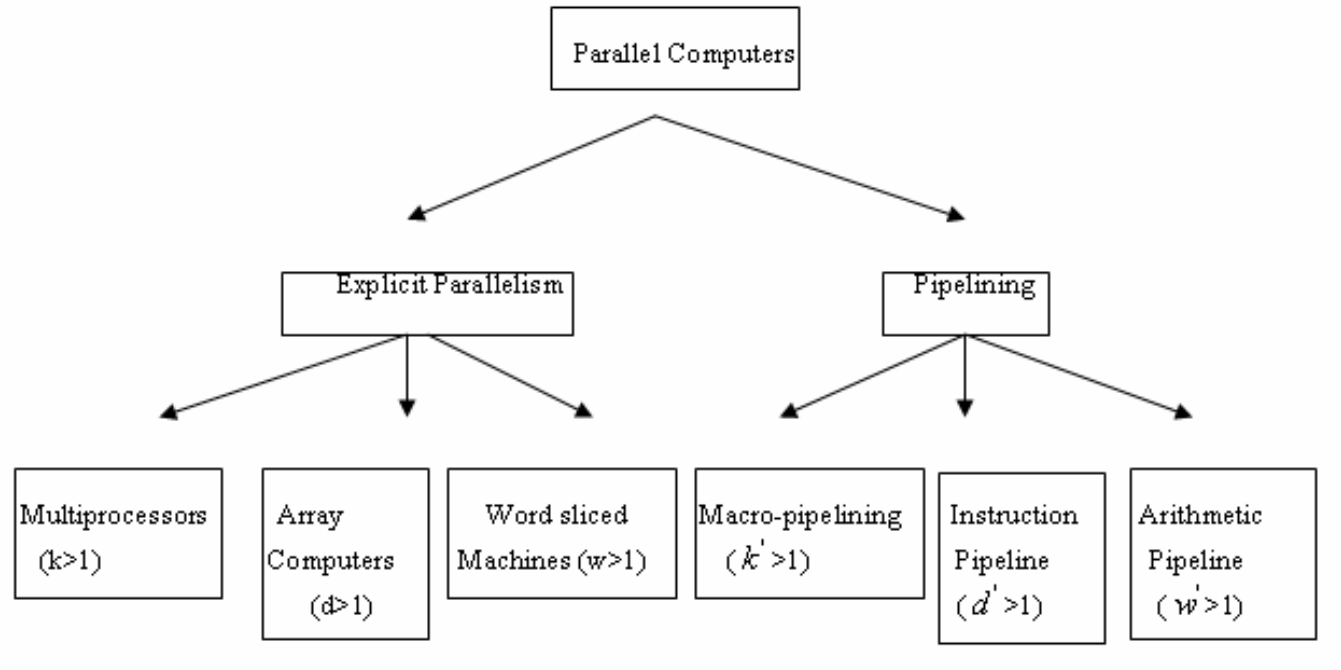
			EXECUTION STREAMS			
			SINGLE		MULTIPLE	
			SCALAR	ARRAY	SCALAR	ARRAY
INSTRUCTION STREAM	SINGLE	SCALAR	Uniprocessor	Uniprocessor	SIMD	
		ARRAY		ILLIAC-IV		
	MULTIPLE	SCALAR			NYU Ultracomputer	Cray X MP
		ARRAY				

11.2 Classification of Computer Architectures

- Hwang & Briggs Classification Scheme:
  - The main new contribution of the classification due to Hwang & Briggs is the introduction of the concept of *classes*.
  - This is a further refinement on Flynn's classification.
  - The SISD category is further refined into two sub-categories, i.e. single functional unit SISD (SISD-S) and multiple functional units SISD (SISD-M).
  - The MIMD category is further refined into loosely-coupled MIMD (MIMD-L) and tightly-coupled MIMD (MIMD-T).
  - The SIMD category is further refined into word-sliced processing (SIMD-W) and bit-sliced processing (SIMD-B).

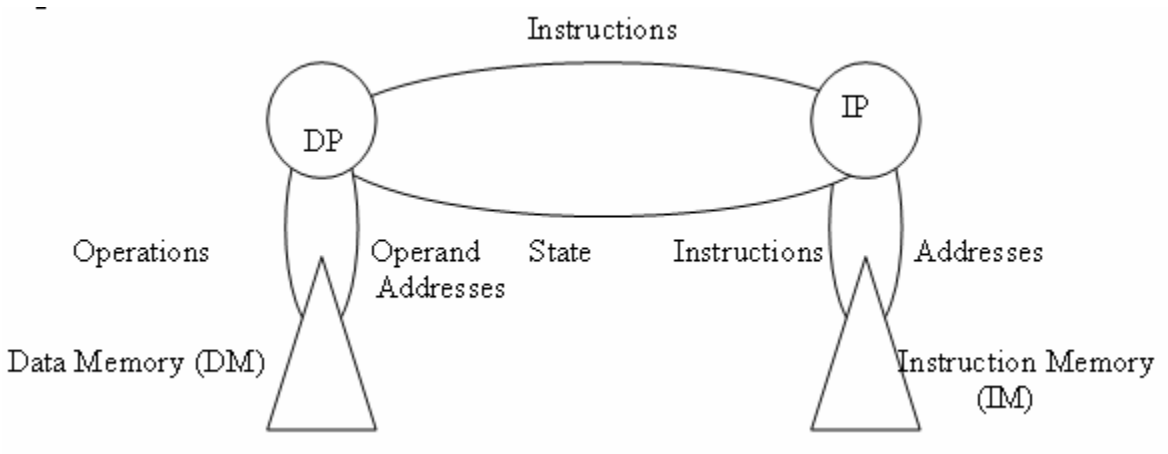
11.2 Classification of Computer Architectures

- Erlangen Classification Scheme



11.2 Classification of Computer Architectures

- Skillicorn Classification Scheme
  - According to this classification, an abstract von Neumann machine is modeled:



11.2 Classification of Computer Architectures

- Skillicorn Classification Scheme
  - Possible connection schemes:

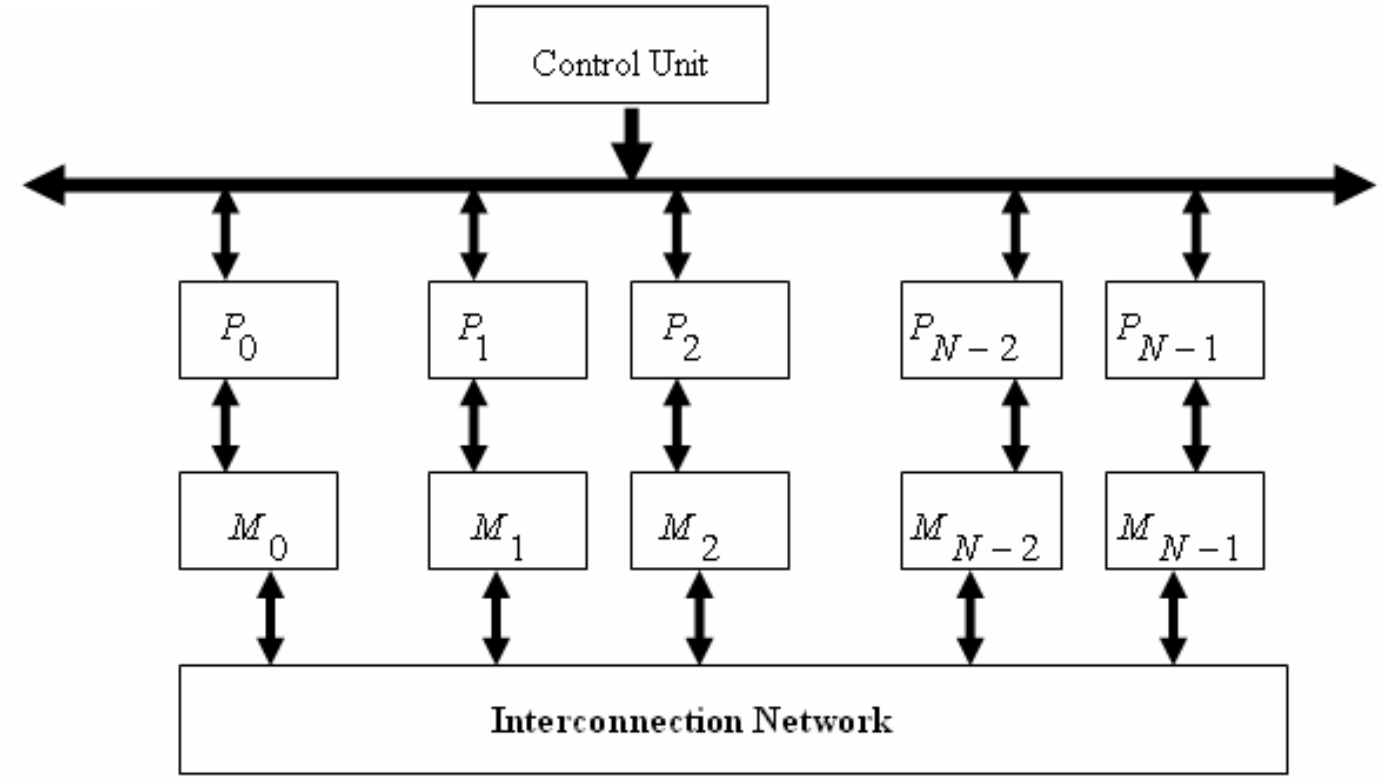
Connection type	Meaning
1-1	A connection between two single units
1-n	A connection between a single unit and *n* other units
n-n	*n* (1-1) connections
n×n	*n* (1-*n*) connections

  - Sample connection classes:

Class	IP	DP	IP-DP	IP-IM	DP-DM	DP-DP	Description	Flynn
1	1	1	1-1	1-1	1-1	None	Von Neumann uniprocessor	SISD
2	1	N	1-n	1-1	n-n	n×n	Type 1 Array Processors	SIMD
3	1	N	1-n	1-1	n×n	None	Type 2 Array Processors	SIMD
4	N	N	n-n	n-n	n-n	n×n	Loosely-coupled von Neumann	MIMD
5	N	N	n-n	n-n	n×n	None	Tightly-coupled von Neumann	MIMD

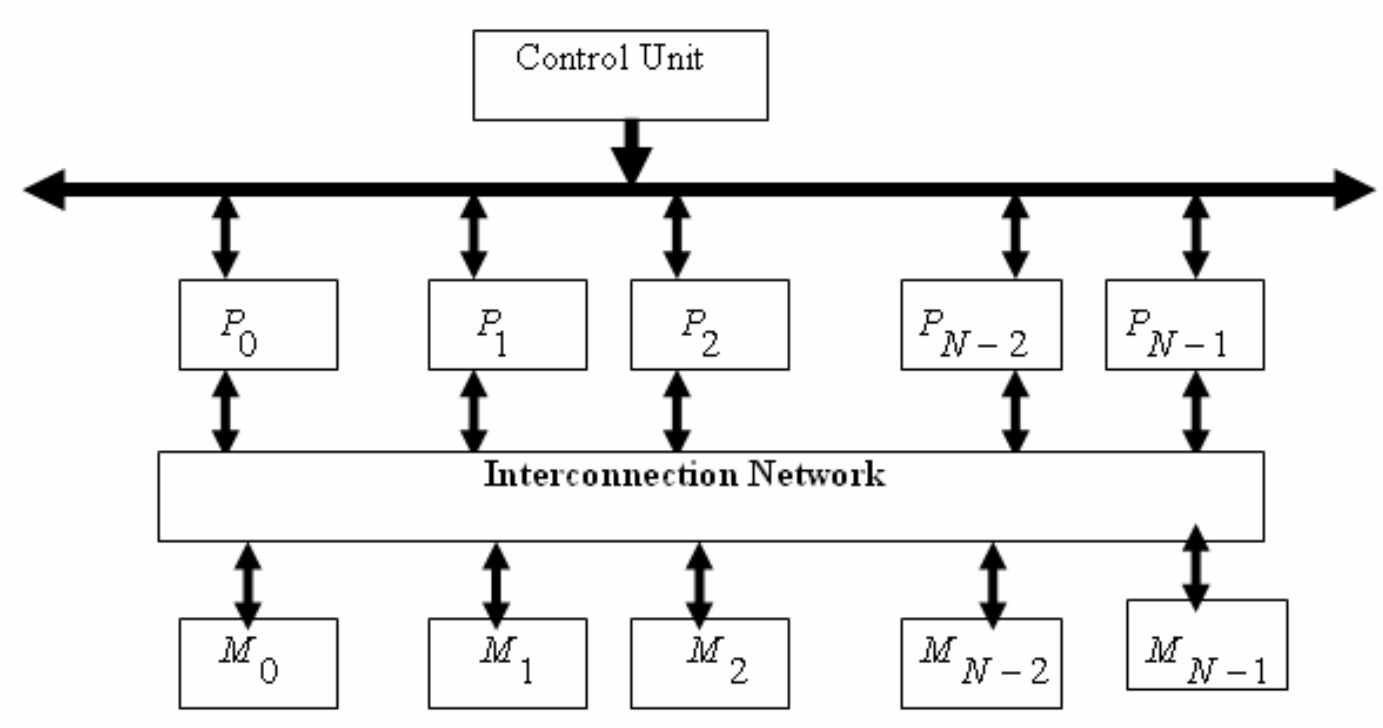
11.3 SIMD Schemes

- First Possible Scheme:



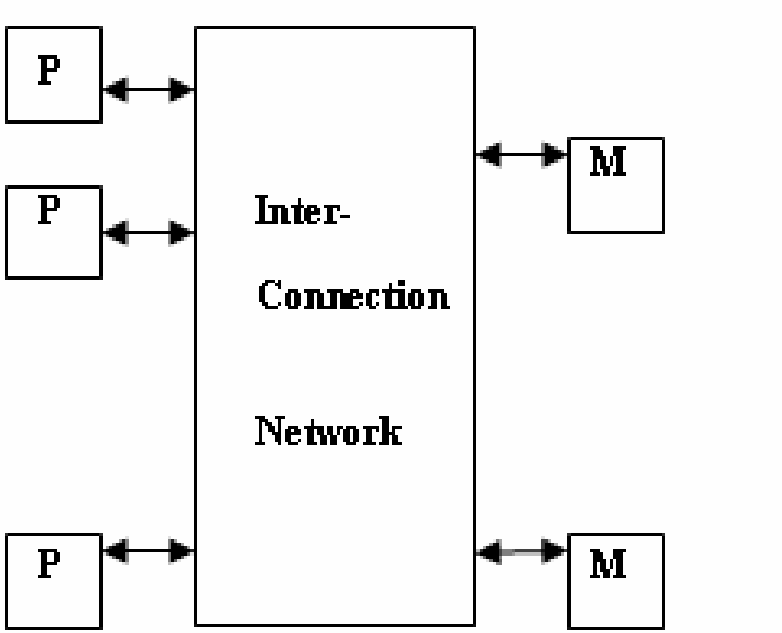
11.3 SIMD Schemes

- Second Possible Scheme:



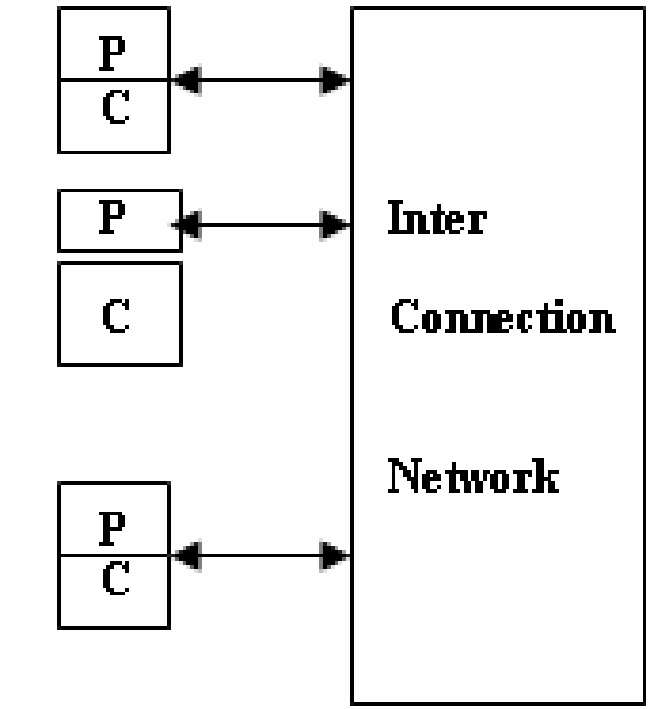
11.4 MIMD Schemes

- Shared Memory Organization
  - Shared memory architecture with a uniform memory access (UMA)



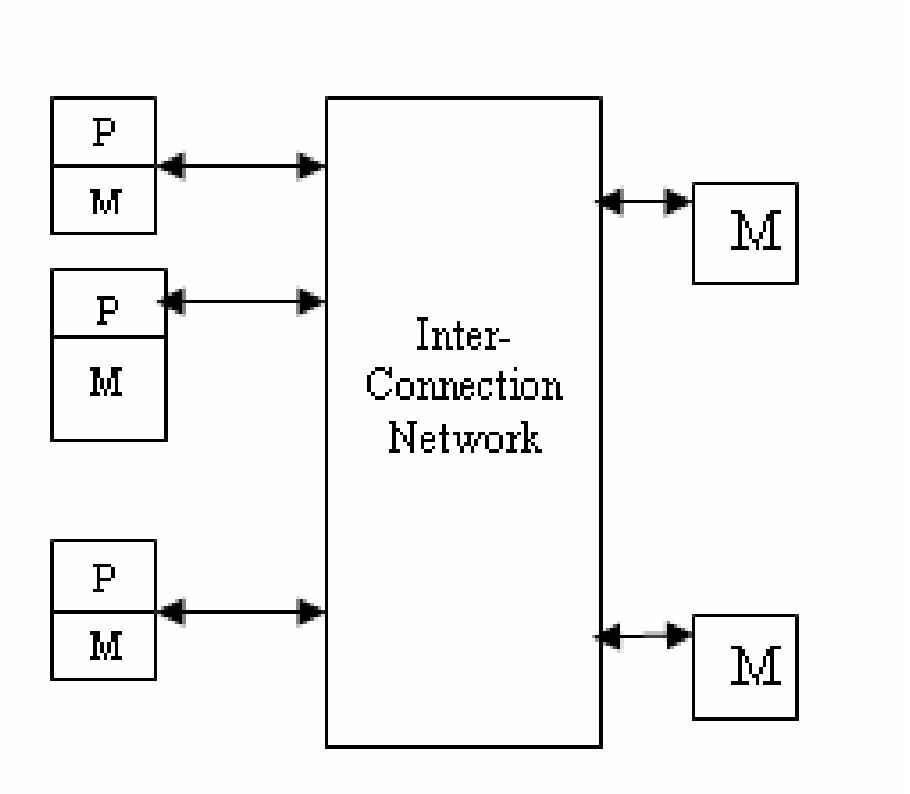
11.4 MIMD Schemes

- Shared Memory Organization
  - Cache-only memory Architecture (COMA)



11.4 MIMD Schemes

- Shared Memory Organization
  - Distributed shared memory architecture with non-uniform memory access (NUMA).

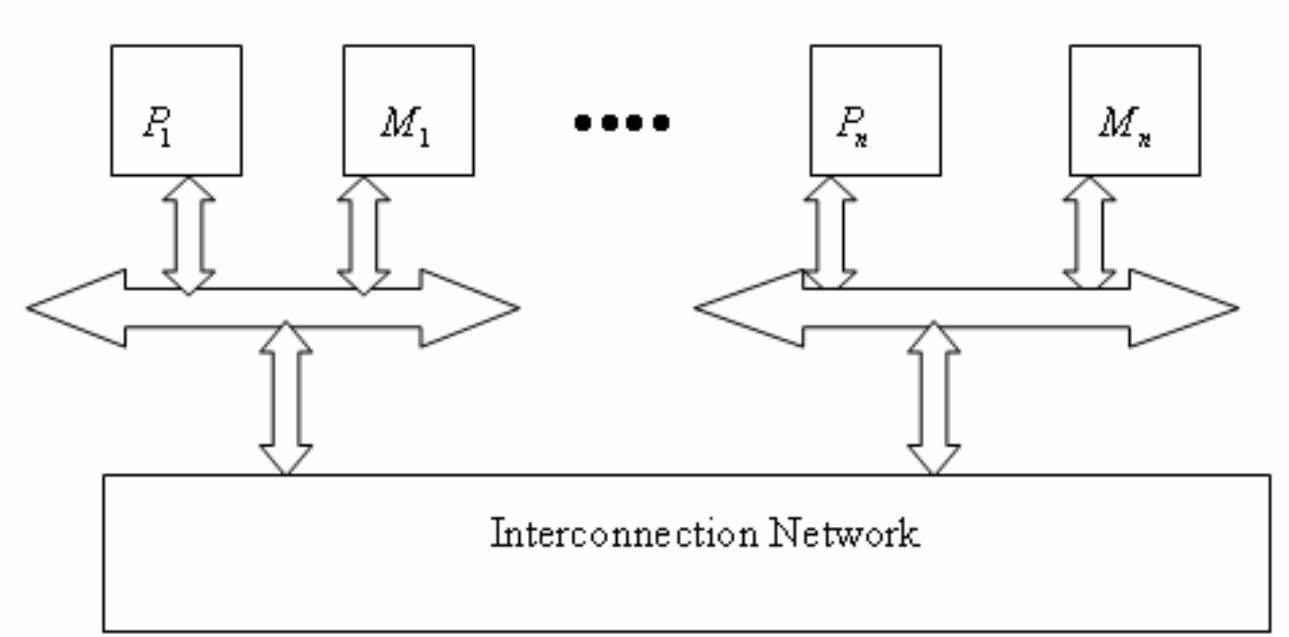


11.4 MIMD Schemes

- Message-Passing Organization
  - Message passing represents an alternative method for communication and movement of data among multiprocessors.
  - Local, rather than global, memories are used to communicate messages among processors.
  - A message is defined as a block of related information that travels among processors over direct links.
  - Examples of message passing systems include the cosmic cube, workstation cluster, and the transputer.

11.4 MIMD Schemes

- Message-Passing Organization



11.5 Interconnection Networks

- Mode of Operation
  - Synchronous:
    - A single global clock is used by all components in the system (lock-step manner)
  - Asynchronous:
    - No global clock required
    - Hand shaking signals are used to coordinate the operation of asynchronous systems.

- Control Strategy
  - Centralized: one central control unit is used to control the operations of the components of the system.
  - Decentralized: the control function is distributed among different components in the system.

11.5 Interconnection Networks

- Switching Techniques
  - Circuit switching: a complete path has to be established prior to the start of communication between a source and a destination.
  - Packet switching: communication between a source and a destination takes place via messages divided into smaller entities, called packets.

- Topology
  - Describes how to connect processors and memories to other processors and memories.
  - Static: direct fixed links are established among nodes to form a fixed network.
  - Dynamic: connections are established when needed.

11.6 Analysis and Performance Metrics

- In executing tasks (programs) using a multiprocessor, it may be assumed that a given task can be divided into *n* equal subtasks each can be executed by one processor.
- Therefore, the expected speedup will be given by the efficiency *E(n)=100%.*

$$S(n) = \text{Speed - up factor}$$
$$= \text{increase in speed due to the use of a multiprocessor system consisting of n processors}$$
$$= \frac{\text{Execution time using a single processor}}{\text{Execution time using } n \text{ processors}}$$

$$E(n) = \text{Efficiency}$$
$$= \frac{\text{S(n)}}{\text{n}} \times 100\%$$

11.7 Summary

- In this chapter, we have navigated through a number of concepts and system configurations related to the issues of multiprocessing.
- In particular, we have provided the general concepts and terminology used in the context of multiprocessors.
- A number of taxonomies for multiprocessors have been introduced and analyzed.
- Two memory organization schemes have been introduced:
  - Shared-memory
  - Message passing
- In addition, we have introduced the different topologies used for interconnecting multiple processors.