
CSE 20221: Logic Design

**Adder / Subtractor
Lab Project**

Problem Statement

- Design a digital logic circuit and prototype your design on the Basys board that will show the result on a seven-segment display of the hexadecimal value for the following operations:
 - The sum of two 4-bit binary numbers A and B
 - The subtraction of B from A using two's complement addition
 - The value of A or B
 - The value of A and B

Specifications

- The four pushbuttons on the Basys board are to be used to determine which one of the four results listed above is displayed. The following information describes the specification for displaying the values:
 - BTN0 – The sum of two 4-bit binary numbers A and B
 - BTN1 – The subtraction of B from A
 - BTN2 – The value of A or B
 - BTN3 – The value of $A \cdot B$

Priority Encoding

- If more than one pushbutton is pressed at a time, then set the display based on the highest numbered button that is pressed. For example, if BTN0 and BTN2 are both pressed, then display the value of A or B. If no buttons are pressed, the display should be blank.

Additional Specifications

- The four leftmost switches (SW7 – SW4) on the Basys board shall represent the values for A.
- The four rightmost switches (SW3 – SW0) shall represent the values for B.
- You may ignore any results due to arithmetic overflow.

Design Procedure Requirements

- Follow the design steps previously outlined in a class lecture.
- The design must be organized in a top-down hierarchical format.
- The top level schematic shall be primarily composed of user-defined symbols.
- User-defined symbols are generated from separate schematics.
- Circuits must be designed using individual logic gates and multiplexers and demultiplexers. No packaged devices such as an adder are allowed.

Design Process Deliverables

- A written introduction and interpretation of the problem.
- An identification of inputs and outputs with a description of their function.
- A top-level view of the design (block diagram).
- Design artifacts such as function tables, Karnaugh maps, schematics and any other pertinent notes.
- Simulation results along with pertinent annotations. You should simulate individual blocks and verify correct functionality before you simulate the entire design.

Design Process Deliverables

- A working prototype that verifies and validates the correct functionality.
- A written summary of the outcome of the project and any problems that were encountered.

Due Dates

- **Week of February 15** — Demonstrate during your lab session that you are able to display four different values using the pushbuttons. The source of your hex values can come from the 8 switches and / or from constant wired values using gnd and vcc. Also, demonstrate that your priority encoding scheme works. (10 points)
- **Week of February 22** — Demonstrate that your prototype meets the design specifications. (20 points)
- **March 4** — Turn in a written report that includes all the deliverables noted in the design process section except the working prototype. Your report must be well organized and presented in a professional manner. (30 points)

This requirement has been recinded.

Lab Partners

You are encouraged but not required to work with another person enrolled in the course. If you have a lab partner you should only submit one written report

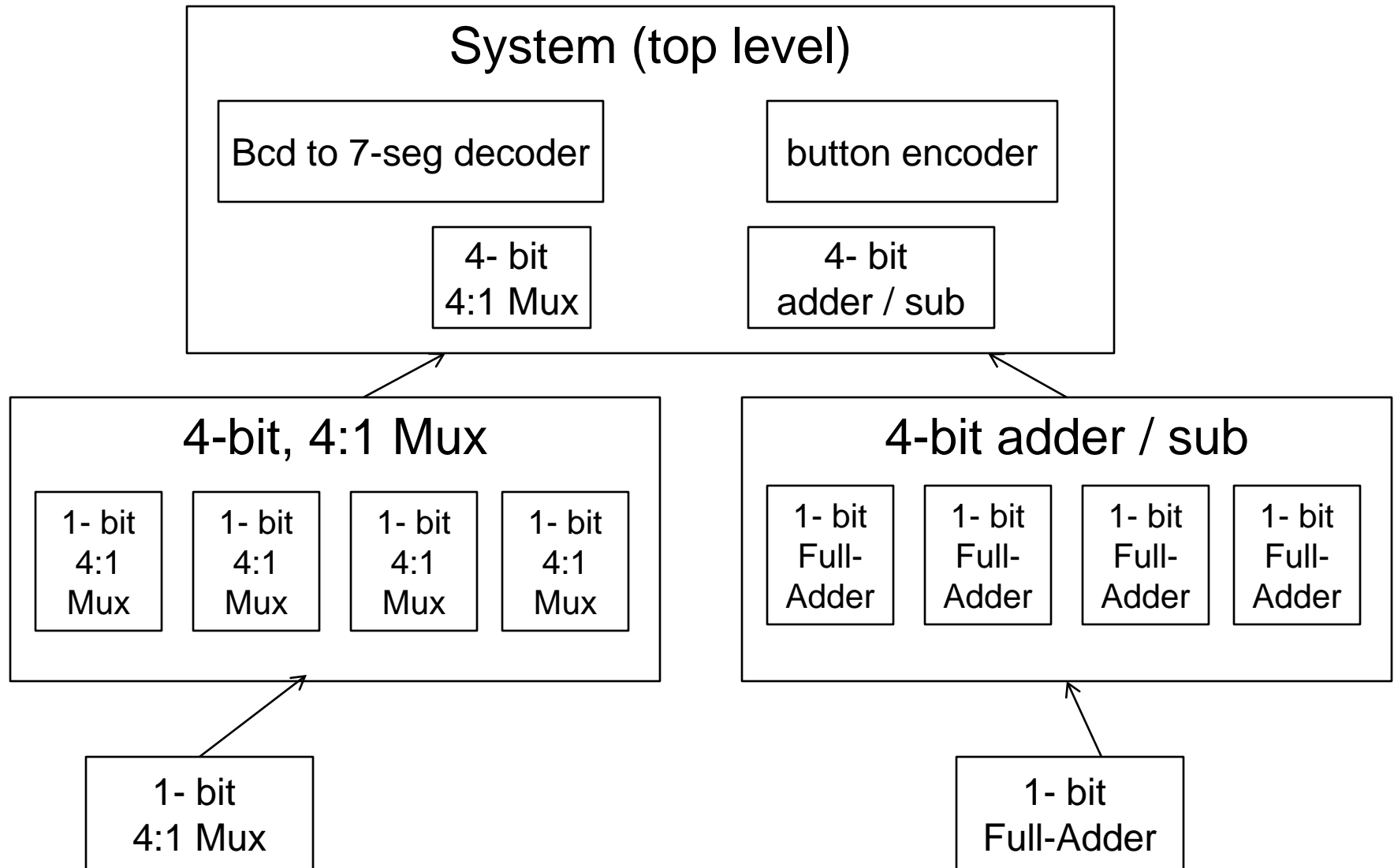
Hierarchical Design Using Xilinx ISE

- Create a schematic for each major function, e.g.
 - 1-bit 4-to-1 multiplexer, full-adder
- Create test bench and verify correct simulation
- Create a symbol for low level schematic
 - In schematic source file specify implementation
 - In process window expand Design Utilities
 - Double click on Create Schematic Symbol
 - Save the symbol with a descriptive name
- Scale up low level objects, e.g.
 - Make 4-bit adder by using 4 full-adders
 - Make 4-bit, 4-to-1 multiplexer using 1 bit mux

Using User-Defined Symbols

- User-Defined symbols are just like logic symbols
- Adding symbol to higher level schematic:
 - First create a new schematic for the higher level
 - In the sources categories window select the folder where you stored the previously made symbol
 - Select the desired symbol and drop on to the schematic

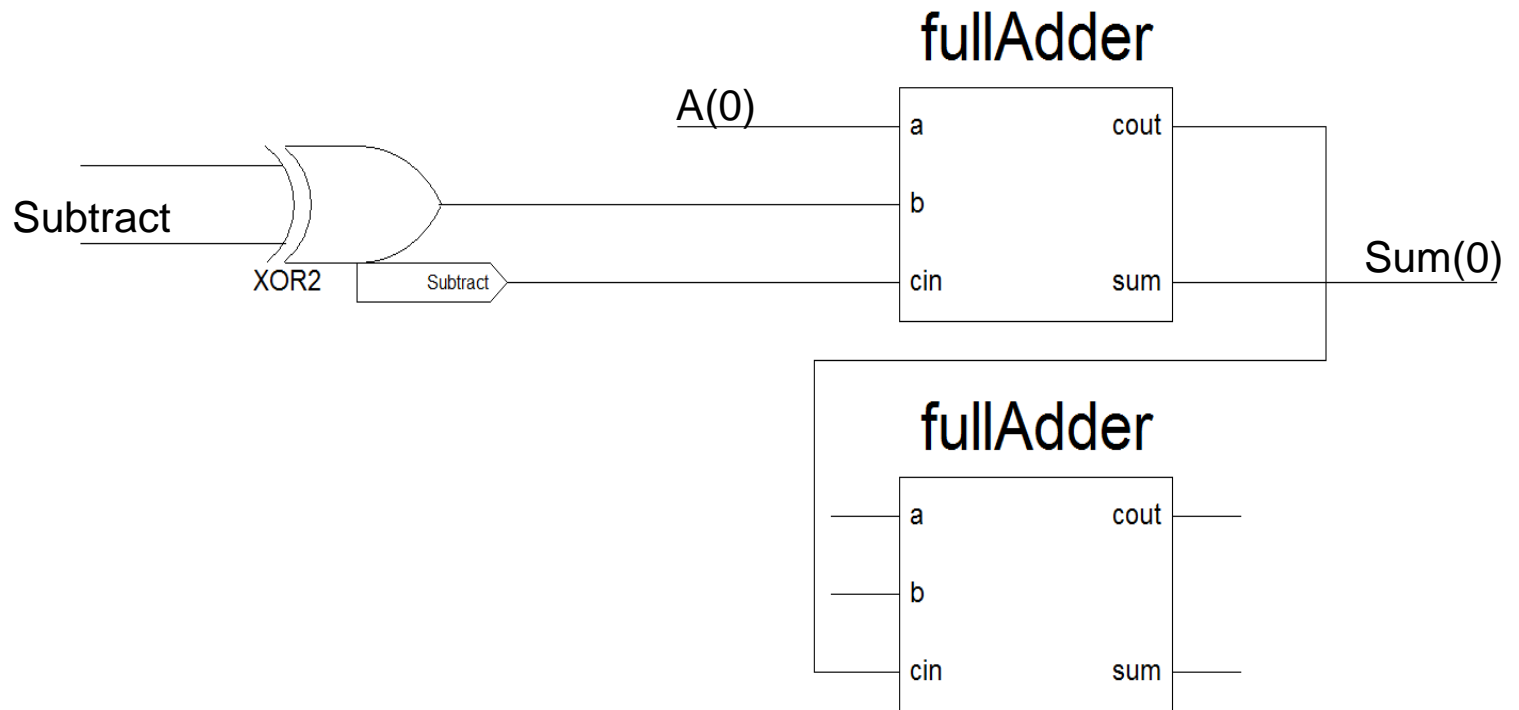
Hierarchical Example



Some Useful Schematic Editor Notes

- Tools: check schematic (do before simulation)
- Sources: general categories: gnd (“0”), vcc (“1”)
- Help (make use of the help menu)
- Display net (wire) name (for ease of readability)
 - right click net
 - select add under visible column
 - select location and locate name at desired position
- Use names to connect nets instead of wire
 - select Add – Net Name
 - name and place on net
 - connect to another net by using the same name

Using Names to Connect Nets



Some Useful Schematic Editor Notes

- Use busses when multiple wires make up a single entity, e.g.
 - 16-bit adder: $a_{15} .. a_0 \Rightarrow A$
- View *Using Busses* under the video section of the course web site

Xilinx Schematic Bus Exampe

